Intelligent Sensors - Overview, Design Hints and Examples

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The common way of connecting analog sensors to P-NET (or to other fieldbus systems) is to take a coupling box with a P-NET port on one side and various analog inputs on the other. Typically for such modules in the P-NET world is the availability of additional process functions allowing the implementation of local process algorithms. Because of decreasing costs for coupling hardware like microcontrollers there is a trend towards so called intelligent sensors with on-board P-NET coupler. Although „smart sensor“ seems to be the better name we should speak of an „intelligent sensor“ because „smart“ usually stands for devices with so called HART protocol being not a real fieldbus but a 4...20 mA interface with low speed binary signals in superposition.

1. Intelligent Sensors: Structures and Requirements (Figures 1-3)

Fig. 1 shows the basic structure of an intelligent sensor. Analog Signal Conditioning in this context means circuits like amplifiers, filters etc. After an Analog Digital Conversion (ADC) the process value is stored inside the memory of a controller (typically micro controller) where also some digital signal conditioning algorithms may run. Via a bus coupling device the value or a value being calculated can be read out from the bus.

Whereas conventional sensors only support data traffic in one direction - from the sensor to the host or to the coupling fieldbus box - intelligent sensors allow data to be send in both direction. Not only pure process data is sent but also derived data, status information and various parameters (*Fig. 2*). Looking on typical bus structures within the area of process industry leads to the requirements shown in *Fig. 3*. One can recognize that P-NET completely fulfills those requirements. In accordance to Fig. 3 P-NET has the following characteristics:

- access time: 2.8 ms
- about 300 analog transfers per s can be handled
- length of data package: 1...63 bytes within one frame, more with LONG commands
- up to 125 nodes within single P-NET segment, more with multi-segment structure

2. Main Function Blocks (Figures 4-6)

Function blocks in the analog part of the intelligent sensor are shown in *Fig. 4*. Very often voltage output is used where an amplifier is producing a signal correlated to the input range of the ADC. Instead of this it may be cheaper and more accurate in many cases to take an oscillator circuit with the sensor’s resistor, capacity or inductance as frequency determining element. In *Fig. 5* the ADC methods for the two basic output signals of the analog part are described. For frequency signals two internal timers of the micro controller can be used to measure the frequency.

Fig. 6 is showing three possible structures of combining the controller and the bus coupler. In the P-NET world of today the standardized method is to take a 8 bit micro controller with integrated UART. Whereas the controller then calculates all procedures of layer 2 and 7 of the P-NET protocol - the main layers for slave implementations - an external driver is used for implementing layer 1. Another method can be to take a micro controller with external P-

NET protocol chip and driver. Or - for very simple sensors - one take a special programmable fieldbus chip (IX-1) as single chip solution.

3. Cost-effective Implementation of P-NET

In this chapter the above mentiond three methods of implementing P-NET into a sensor will be described.

When using the first method - called software protocol - the UART of the micro controller should be configured in a way that it will produce an interrupt on signal „1“ of the 10th bit of the frame because this is the address/data bit signalling that the first 11 bit group of the master request frame is coming in (*Fig. 7*). Then the complete rest of the frame will be read in within the Interrupt Service Routine (ISR) followed by the building up of the response frame. Of course when the first 11 bit group representing the slave node adress is not identical to the sensor’s address the ISR can be finished very fast.

The timing requirements being a little bit critical because of the need for immediate response are listed in *Fig. 8*.

When using the P-NET Chip (PNC) like shown in *Fig. 9* the data handling can be controlled by interrupt leading to a lower controller load for managing the fieldbus traffic (*Fig. 10*). From P-NET side some Softwire Numbers are predefined (*Fig. 11*). Others can be defined and handled within the host CPU.

Taking the IX-1 (designed by DELTA t, produced by SGS-Thomson) means that the P-NET protocol has to be loaded into a serial (EE)PROM from which it can be read in into the IX-1 internal program memory after reset (*Fig. 12*). Of course an additional RS-485 driver must be used. The register model in *Fig. 13* shows that the IX-1 has a so called Harvard architecture with programm and data memory physically decoupled. In *Fig. 14* the principal coupling of the application - being ADC and sensor device with analog hardware - is shown.

Of course when developping intelligent P-NET sensors the rules for designing the channels and registers must be followed too. The minimum solution being in accordance to the „Standardized General Purpose Channel Types“ (published by the International P-NET User Organization) is defined in *Fig. 15*. In many cases it is possible to add some more process functions like PID or Fuzzy Control etc. without any new hardware. Then additional channels must be defined.

4. Examples from P-NET World

In *Fig. 16* some examples of intelligent P-NET sensors being on the market for a longer time are given. Here intelligent sensor means that the complete electronics including all P-NET coupling devices are inside the housing of the sensor. In addition there are many other sensors with external electronic box including the P-NET interface available. Specialized coupling devices making a conventional sensor intelligent - but not having a real intelligent sensor then - are listed in part B) of Fig. 16.

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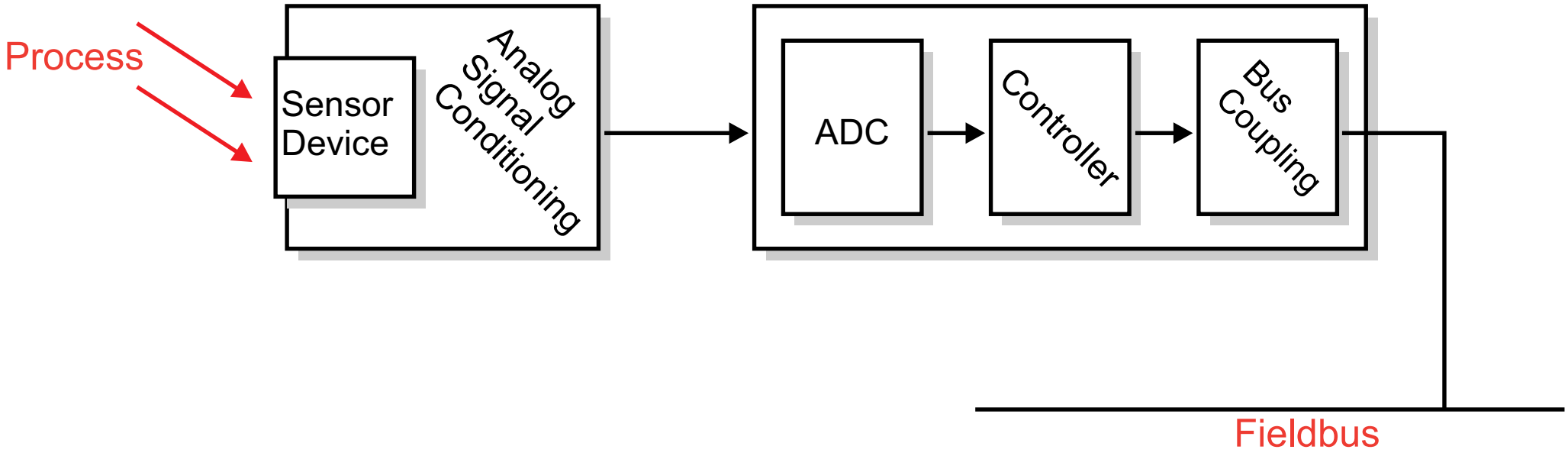
Basic Structure of Intelligent Sensors



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Communication Data

From Sensor:

- Process Data (e.g. Pressure, Temperature, Humidity, ...)
- Derived Data (e.g. Average, Integral: Flow from Speed etc., Output of PID Algorithm, ...)
- Status (e.g. Fault Messages, Self Monitoring, etc.)

To Sensor:

- Parameter for Digital Signal Conditioning (Linearization, Compensation of Temperature, Manufacturing Jittering, ...)
- Parameter for the Calculation of Derived Process Data
- Bus specific Parameters (e.g. Node Address, ...)

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Requirements on the Fieldbus System

E.g. Intelligent Sensors for analog Process Data in Process Industry:

Single Sensor:

- Access Time: max. 10 ms
- Time Gap between two Accesses changeable: typ. 100 ms (e.g. fast Measurements of Flow) ... 1 min (Monitoring of Temperature)
- Length of Data Package changeable: 1 Byte (e.g. Error Status) ... 4 Byte (e.g. Process Data) ... 1 kByte (e.g. Complete Signal Conditioning Algorithms)

Whole System:

- typ. up to 50 Bus Nodes
- Data Through Put: typ. up to 100 Process Data per s

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Analog Signal Conditioning

- Sensor Device Output:

  A) In most cases: Impedance (Resistor, Capacity, Inductance)
  B) Sometimes: Electrical Charge (Piezo Sensor), Voltage (Thermo Couple)

- Signal Conditioning for Type A):

  - D.C. or A.C. Bridge with Voltage Output, if need be A.C./D.C. Converter, D.C. Amplifier (Voltage to Voltage)
  - Oscillator with Frequency Output

- Signal Conditioning for Type B)

  - D.C. Amplifier (Charge/Voltage to Voltage)

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Analog Digital Conversion

- ADC for Frequency Signals:

  Algorithm for Frequency Measurement within the Micro Controller

  - Lower Frequencies: Time Measurement of 1 Period or n Periods, f = 1/T
  - Higher Frequencies: Counting of Periods per $T_{measure}$ = const.
  - Resolution Changeable by Parameters n or $T_{measure}$ (typ. 10, 12, 14, 16, 18 Bit)

- ADC for Voltage Signals:

  External or built-in Converters

  - Various Methods (very often: Successive Approximation, Sigma-Delta)
  - Resolution in most cases fixed (typ. 8, 10, 12, 14 Bit)

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Controller & Bus Coupling

- Micro Controller with P-NET Software Protocol

  - typ. 8 Bit type with integrated UART (8051, 6805, 68HC11, ...)
  - UART should be able to initiate Interrupt on 10th bit (adress/data bit of the P-NET frame)
  - external RS-485 driver, galvanically decoupled (see standard)

- Micro Controller with external P-NET Protocol Chip

  - P-NET Chip (PNC) and RS-485 driver or
  - IX-1 with P-NET firmware

- Single Chip Solution

  - IX-1 with P-NET firmware (including application)

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Software Protocol (Flow Chart)

Interrupt from UART on 10th Bit (Address/Data Bit is 1)

Interrupt Service Routine:

Master Request

Read in Slave Address

If Slave Adress <> Own Address RETI

Read in Master Address

Read in Control

Read in Info Length and Info Field

Read in and proof Checksum

Case
LOAD/
LONG LOAD:
: - if need be call service routine (e.g. for transformation internal data format into P-NET data type)
- send out response frame
- RETI

others
: - if TAS: make TAS operation
- send out response frame
- put adress of service routine on stack and RETI
- call service routine (e.g. for transformation P-NET data type into internal format)
- RET

Slave Response

Back to Main Routine

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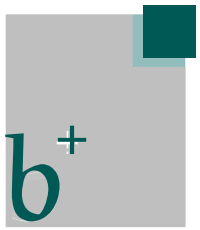

Software Protocol (Timing Requirements)

Two basic Limits:

- Slave must not answer before 11 Bit Periods after Receiving of the last Bit of the Master Request
- Slave must answer not later than 30 Bit Periods after Receiving of the last Bit of the Master Request

With P-NET Bitrate 76.800 Bit/s (1 Bit about 13 µs):

11 Bit: 143 µs 30 Bit: 390 µs

Typically a Timer is used for Supervision

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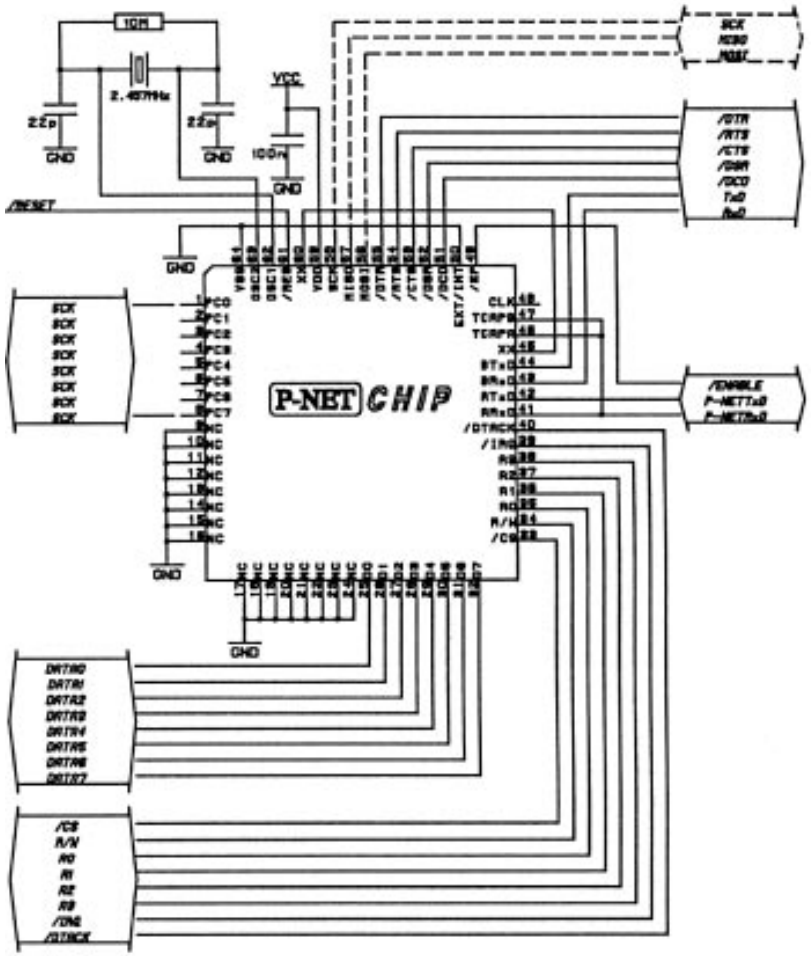
Hardware Protocol (P-NET Chip)

Structure:



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Hardware Protocol (P-NET Chip)

Data Handling:

- P-NET Chip (PNC) receives Request Frame from Master and built up Slave_Request_Packet
- Slave_Request_Packet is put into Slave_Request_FIFO (Depth is 4 Bytes)
- Host CPU reads out Slave_Request_FIFO whenever it is full and the PNC has generated Interrupt ("FIFO full")
- After receiving the complete Packet the Host CPU has to built up Slave_Response_Packet
- Host CPU sends Slave_Response_Packet to PNCs Slave_Response_FIFO; controlled by interrupt ("FIFO empty")
- PNC sends out Response Frame

Ckecksum managed by PNC

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Hardware Protocol (P-NET Chip)

Registers:

To P-NET

SWNo	Register
01	ModePort1
02	ModePort2
03	DigIO Port_C Data
04	DigIO Port_C Data_Direction
05	Handshake Port
06	RTC
07	EEPROM

To Host CPU

Reg.No	Register
00	FIFO_Out_A
01	FIFO_Out_B
02	FIFO_Out_C
03	FIFO_Out_D
04	FIFO_In_A
05	FIFO_In_B
06	FIFO_In_C
07	FIFO_In_D
08	FIFO_A_Status
09	FIFO_B_Status
0A	FIFO_C_Status
0B	FIFO_D_Status
0C	Interrupt_Status
0D	Interrupt_Mask
0E	Mode
0F	(unused)

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Minimum Registers for an Intelligent P-NET Sensor

Service Channel (Channel 0)

SWNo	Identifier	Type
00	NumberOfSWNo	Integer
01	DeviceID	Record
04	PNETSerialNo	Record
0D	WriteEnable	Boolean
0E	ChType	Record
0F	CommonError	Record

Analog Channel (Channel 1)

SWNo	Identifier	Type
10	AnalogIn	Real
19	ChConfig	Record
1B	Fullscale	Real
1C	Zeropoint	Real
1D	Maintenance	Record
1E	ChType	Record
1F	ChError	Record

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Some Intelligent Sensors from P-NET World

A) *Intelligent Sensors*

Manufacturer	What is measured ?
PROCES-DATA	Flow
ULTRAKUST	Humidity, Temperature (with/without contact), Flow
INFRA SENSOR	Temperature (without contact)
Perhaps You !	XYZ

B) *Intelligent P-NET Coupling Devices for analog Sensors*

E.g. from PROCES-DATA, ULTRAKUST, IPH Marine Automation, Tilse, ...

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Designing an Application with IX1

Application Program
(e.g. periodically Initiation of AD-Conversion, Conversion into real format, ...)

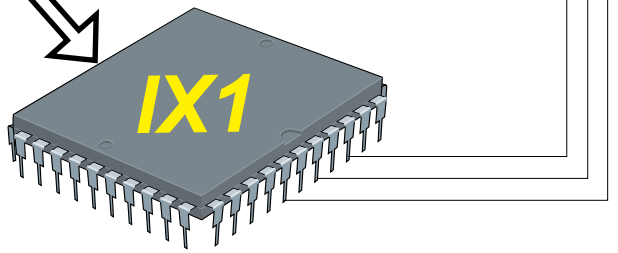
Driver Protocol

Library Functions
(e.g. Mathematics, Debugging, ...)

Developped with IX1-Forth or -C Prototyping System

Compilation → IX1-Object Code → *e.g. Burning, Download* → serial (EE)PROM

Application Hardware



Bus

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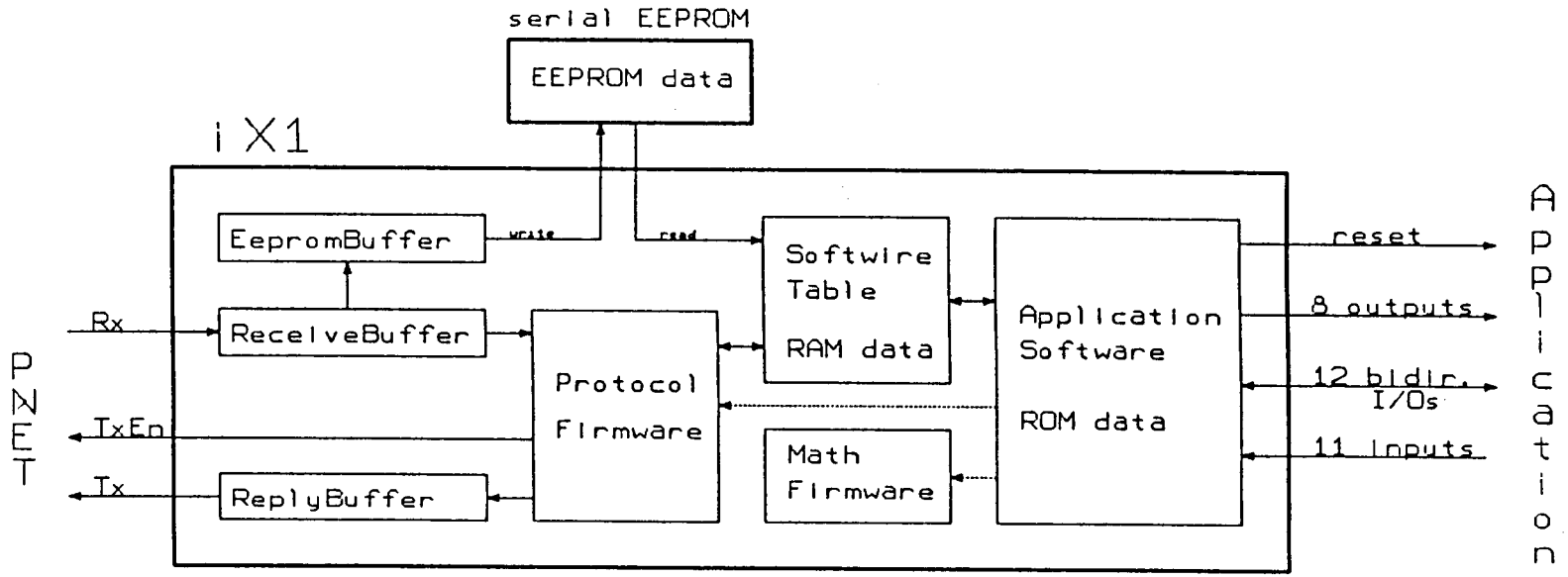
Example: Block Diagram P-NET Single-Chip Slave



Drawing by DELTA t, Hamburg

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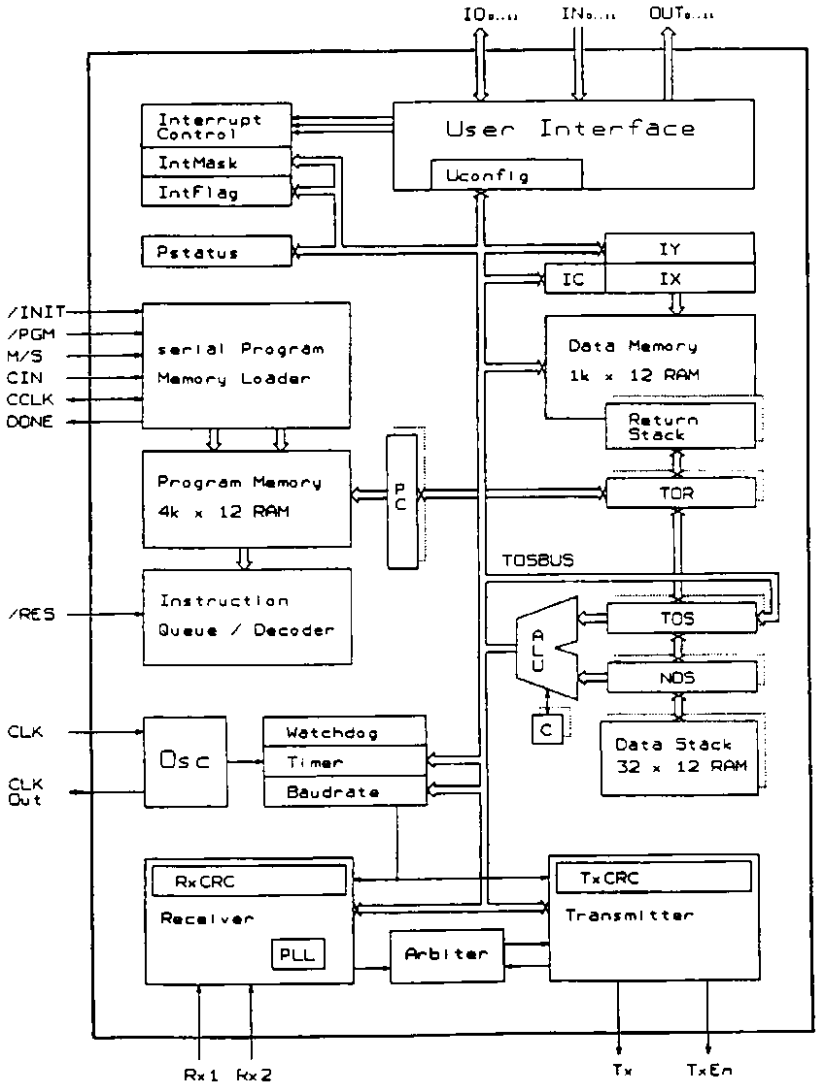
Register Model of the IX1



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